REMARKS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-62 are pending in the present application. Claims 1, 3, 5, 32, 34 and 36 have been amended, and Claims 61 and 62 have been added by the present amendment.

In the outstanding Office Action, the drawings and Claims 1 and 5 were objected to; Claims 1, 3, 5, 7, 11, 14, 34 and 36 were rejected under 35 U.S.C. § 103(a) as unpatentable over Applicants' Admitted Prior Art (AAPA) in view of Tomioka et al; and Claim 32 was rejected under 35 U.S.C. § 103(a) as unpatentable over AAPA in view of Tomioka et al and Kim et al.

Regarding the objections to the drawings and Claims 1 and 5, Figures 46A, 46B, 47A, 47B, 48A, 48B, 49A and 49B have been labeled "Related Art" in light of the comments noted in the outstanding Office Action. A separate letter requesting approval of drawing changes is being submitted to the draftsman. In addition, Claims 1 and 5 have been amended in light of the comments noted in the outstanding Office Action and as shown in the marked-up copies. It is believed no new matter has been added. Accordingly, it is respectfully requested the objections to the drawings and Claims 1 and 5 be withdrawn.

Claims 1, 3, 5, 7, 11, 14, 34 and 36 were rejected under 35 U.S.C. § 103(a) as unpatentable over AAPA in view of Tomioka et al. This rejection is respectfully traversed.

Claim 1 is directed to a semiconductor device including a first electrode layer formed on a first insulating film and a second electrode layer formed on a second insulating film and an exposed surface of a first electrode layer, with a second electrode layer electrically connected to the first electrode layer via an open portion. The first and second electrode layers include a gate electrode, and the open portion has a first width in a direction of a gate

length of the gate electrode and a second width in a direction perpendicular in the direction of the gate length, in which the second width is greater than the first width.

In a non-limiting example, Figures 2 and 3 show that in the open portion 17 of the insulating film 16, the length of the open portion 17 in a direction perpendicular to the direction of the gate length L is large, although the width of the open portion 17 in the direction of the gate length L is small. As a result, resolution is facilitated in the lithography process in patterning the open portion 10. Accordingly, even when the gate length L is small, it is possible to finely form an open portion 17 (see the specification at page 29, lines 16-27).

By contrast, Tomioka et al merely describe applying patterning to a photoresist after the photoresist is applied all over a surface, so that a part of an ONO film on a select transistor side is removed, and a part of the ONO film on the select transistor side is removed by etching to form an opening (see column 10, lines 9-15). However, Tomioka et al do not teach or suggest an open portion that has a first width in a direction of a gate length of a data electrode and a second width in a direction perpendicular to the direction of the gate length, and in which the second width is greater than the first width, as in Claim 1. Further, Tomioka et al do not disclose a shape of an open portion at all. AAPA also does not teach or suggest these features.

Accordingly, it is respectfully submitted independent Claim 1 and each of the claims depending therefrom are allowable.

Claim 32 was rejected under 35 U.S.C.§ 103(a) as unpatentable over AAPA in view of Tomioka et al and Kim et al. This rejection is respectfully traversed.

Claim 32 depends from Claim 1, which as discussed is believed to be allowable. Further, it is respectfully submitted that Kim et al do not teach or suggest the features of independent Claim 1. Accordingly, it is respectfully requested this rejection be withdrawn.

In addition, new Claims 61 and 62 have been added to set forth the invention in a varying scope. In particular, new Claim 61 is directed to a semiconductor device in which an open portion extends over element regions identical to an element region in a direction perpendicular to a length of the gate length, which is supported in the specification at least in Figure 1. Also, new Claim 62 is directed to a semiconductor device in which an element isolating insulating film is provided between element regions and includes a groove formed in the element isolating insulating film, and in which the groove is located under an open portion and has the same shape as the open portion, which is supported in the specification at least in Figure 3B. It is respectfully submitted that AAPA, Tomioka et al, and Kim et al do not teach or suggest the features of new Claims 61 and 62, and new Claims 61 and 62 are believed to be allowable for at least the reasons discussed above.

Further, Claims 1, 5, 32, 34 and 36 have been amended to correct minor informalities and conform to standard claim drafting practice. It is believed no new matter has been added.

Consequently, in light of the above discussion and in view of the present amendment, the present application is believed to be in condition for allowance and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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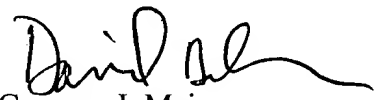

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IN THE CLAIMS

--1. A semiconductor device comprising:

a semiconductor layer;

a first insulating film formed on said semiconductor layer;

a first electrode layer formed on said first insulating [layer] film;

an element isolating region comprising an element isolating insulating film formed to extend through said first electrode layer and said first insulating film to reach an inner region of said semiconductor layer, said element isolating region isolating an element region and being self-aligned with said first electrode layer;

a second insulating film formed on said first electrode layer and said element isolating region, an open portion exposing a surface of said first electrode layer being formed in said second insulating film; and

a second electrode layer formed on said second insulating film and said exposed surface of said first electrode layer, said second electrode layer being electrically connected to said first electrode layer via said open portion, said first and second electrode layers including a gate electrode, said open portion having a first width in a direction of a gate length of said gate electrode and a second width in a direction perpendicular to the direction of the gate length, the second width being greater than the first width.

3. (Amended) The semiconductor device according to claim 1, wherein said [first and second electrodes comprise] gate electrode is a gate electrode of a selective transistor included in a NAND type flash memory.

5. (Amended) The semiconductor device according to claim 1, which is a semiconductor device in a memory cell array region, comprising:

said semiconductor layer;

said first insulating film formed on said semiconductor layer;

said first electrode layer formed on said first insulating [layer] film;

said element isolating region comprising an element isolating insulating film formed to extend through said first electrode layer and said first insulating film to reach an inner region of said semiconductor layer, said element isolating region isolating an element region and being self-aligned with said first electrode layer;

said second insulating film formed on said first electrode layer and said element isolating region; and

said second electrode layer formed on said second insulating film;

wherein a surface of said element isolating region of said memory cell array region is arranged below a surface of said first electrode layer.

32. (Amended) The semiconductor device according to claim 1, wherein an electric resistance of said second electrode layer is lower than that of said first electrode layer, and said second electrode layer comprises [of] a metal layer including a high melting point or a lamination layer film comprising a metal silicide layer including a high melting point and a polysilicon layer.

34. (Amended) The semiconductor device according to claim 1, wherein said second insulating film comprises [of] a complex insulating film including a silicon nitride film.

36. (Amended) The semiconductor device according to claim 1, which is a semiconductor device in which [a gate electrode is formed of said first and second electrode layers, wherein] said second insulating film remains at an edge [potion] portion of said gate electrode.

61-62. (New).--